R20

Code No: R20A0506

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech I Semester Regular Examinations, February 2022

Computer Organization

(CSE, CSE-AI&ML, CSE-CS, CSE-DS)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

1	Explain different functional units of a digital computer with neat sketch. Recall the usage of Signed number representations	**[14M]**
	OR	
2	Recall the Multiplication algorithms used in Computer Arithmetic. Convert the following binary number into decimal & octal number: i) (00010.110)2 ii) (000.10110)2	**[14M]**

SECTION-II

3	List and explain the steps involved in the execution of a complete instruction cycle. List the basic symbols used in register transfer Language	**[14M]**
	OR	
4	Classify different Types of Instructions used in Computer Organization with an example.	**[14M]**

SECTION-III

5	Explain direct and immediate addressing Modes. Differentiate CISC and RISC processors	**[14M]**
	OR	
6	Illustrate the micro-programmed control unit(MCU) with a neat diagram and how instructions will be processed in MCU?	**[14M]**

SECTION-IV

7	Draw a neat block diagram of memory hierarchy in a computer system. Compare the parameters size, speed and cost per bit in the hierarchy.	**[14M]**
	OR	
8	Explain the following mapping techniques used for cache mapping i) Associative mapping ii)Direct mapping iii) set-associative mapping cache	**[14M]**

SECTION-V

9	Write a short notes on Peripheral devices .With a neat sketch explain the working principle of DMA	**[14M]**
	OR	
10	Discuss with neat diagrams, How Hazards improved in Pipelining.	**[14M]**

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R20

Code No: R20A0506

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech I Semester Regular Examinations, February 2022

Computer Organization

(CSE, CSE-AI&ML, CSE-CS, CSE-DS)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

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	OR	
10	Discuss with neat diagrams, How Hazards improved in Pipelining.	**[14M]**

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R18

Code No: R18A0505

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech I Semester Supplementary Examinations, July/August 2021

Computer Organization

(CSE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Answer Any **Five** Questions
All Questions carries equal marks.

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1	a). Explain the bus structure in detail with neat diagram.	**[7M]**
	b). What are the functions of ALU.	**[7M]**
2	Differentiate between fixed point and floating point representation.	**[14M]**
3	Explain various types of computer registers with block diagrams.	**[14M]**
4	Explain various instruction formats and write various instruction formats for X=(A+B)*(C+D).	**[14M]**
5	a). Explain the different Addressing modes with numerical example.	**[7M]**
	b). Discuss CISC and RISC processors.	**[7M]**
6	Illustrate the binary division process through a numerical example.	**[14M]**
7	Explain briefly about memory hierarchy.	**[14M]**
8	With the help of a block diagram. Explain DMA transfer in detail.	**[14M]**

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R18

Code No: R18A0505

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech I Semester Regular/Supplementary Examinations, February 2021

Computer Organization

(CSE)

Roll No										

Time: 2 hours 30 min **Max. Marks: 70**

Answer Any **Five** Questions
All Questions carries equal marks.

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1	a). Explain about data representation.	**[7M]**
	b). With a neat sketch, explain in detail about the functional units of computers.	**[7M]**
2	What is bus? Draw the figure to show how functional units are interconnected using a bus and explain it.	**[14M]**
3	What is Instruction Cycle? Briefly explain with state diagram.	**[14M]**
4	What is the difference between a direct and an indirect address instruction? And Explain about various addressing modes.	**[14M]**
5	Explain clearly three types of CPU organizations.	**[14M]**
6	Draw and explain a flowchart of multiplication algorithm.	**[14M]**
7	Explain the following Auxiliary memory devices: i. Magnetic disks **ii.** Magnetic tape.	**[14M]**
8	Describe in detail about input-output-processor (IOP) organization.	**[14M]**

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Code No: **R18A0505**

R18

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech I Semester Regular Examinations, November 2019

Computer Organization

(CSE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

1	a) Explain the basic operational concepts of a computer with the help of a suitable diagram	**[8M]**
	b) Explain how the performance of a computer is measured	**[6M]**
	OR	
2	a) Use 8 bits to represent -9 in Signed magnitude, Signed 1's Complement, and Signed 2's Complement representations .	**[6M]**
	b) Define a parity bit. Draw the diagrams of 3-bit odd parity generator and checker circuits and explain	**[8M]**

SECTION-II

3	a) Draw and explain the construction of bus system using Three State buffers	**[8M]**
	b) List all the logic microoperations that are performed on the contents of registers	**[6M]**
	OR	
4	a) List and explain the purpose of different registers for the basic computer	**[6M]**
	b) Explain Interrupt Cycle with the help of a flowchart	**[8M]**

SECTION-III

5	a) Compare the hard wired control unit and micro programmed control unit	**[8M]**
	b) Explain about typical Data Transfer Instructions	**[6M]**
	OR	
6	a) Explain the following addressing modes with an example i) Register Indirect Addressing mode ii) Relative Addressing mode	**[6M]**
	b) Discuss about RISC and CISC Characteristics	**[8M]**

SECTION-IV

7	(a) Differentiate Static and Dynamic RAMs	**[6M]**
	(b) Explain Direct mapping technique used for cache mapping	**[4M]**
	(c) What is page fault? List various page replacement algorithms	**[4M]**
	OR	
8	(a) Explain ROM and RAM with respect to their block diagrams	**[7M]**
	(b) Explain how read and write operations are performed in Associative memory	**[7M]**

SECTION-V

9	(a) Describe in detail about IOP organization	**[8M]**
	(b) Explain the method of DMA transfer.	**[6M]**
	OR	
10	Define cache memory? Explain various mapping techniques in cache memory.	**[14M]**

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R18

Code No: R18A0505

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech I Semester Supplementary Examinations, October 2020

Computer Organization

(CSE)

Roll No										

Time: 2 hours **Max. Marks: 70**

Answer Any **Four** Questions
All Questions carries equal marks.
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1 a) Draw the diagram of a Single bus structure and explain.

b) Explain about Multiprocessors and Multicomputer.

2 a) Draw the circuit diagram of 4-bit adder-subtractor circuit and explain its Operation.
b) Explain division algorithms with suitable example.

3 a) Draw and explain 4 bit binary incrementer circuit.
b) Explain the Hardware implementation for generating basic logic micro operations.

4 a) Explain Instruction Cycle with the help of a flowchart.
b) List and explain all the register reference instructions.

5 a) Explain the operation of a Micro programmed control unit using a diagram.

b) Explain the following
i) Micro operation ii) Microinstruction iii) Micro program.

6 a) Draw the block diagram of an 8-bit ALU with a 4-bit status register and explain the purpose of each bit in the status register.
b) Explain about typical Data Manipulation Instructions.

7 (a) Define Hit Ratio.
(b) Explain Write-through and Write-back methods of cache updation.
(c) Implement FIFO algorithm for the following page trace with the frame size 4.
0 1 3 6 2 4 5 2 5 0 3 1 2 5 4 1 0.

8 (a) What is meant by instruction pipeline? Explain four segment Instruction Pipeline. Give its timing diagram.
(b) Discuss briefly the protocols of universal serial bus.

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R17

Code No: R17A0510

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech I Semester Supplementary Examinations, October 2020

Computer Organization

(CSE & IT)

Roll No										

Time: 2 hours **Max. Marks: 70**

Answer Any **Four** Questions
All Questions carries equal marks.

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1 a) Represent the following decimal values as signed 7 bit number using sign magnitude, signed 1's complement and signed 2's complement formats:
i)+43 ii) -10 iii)51 iv)-27
b) Explain the different registers that are available in the processor of a digital computer and the connection between the processor and the memory.

2 a) What are the basic functional units present in the computer and explain each of them?
b) Design a 4 bit Arithmetic Circuit which can perform addition, subtraction, increment and decrement operations.

3 a) Draw the flow chart for interrupt cycle and write in brief about modified fetch phase.
b) Define the following:
i. Microoperation
ii. Microinstruction
iii. Microprogram
iv. Microcode

4 a) What is instruction cycle? Explain various steps involved in the instruction cycle.
b) Write the circuit of Microprogram sequencer for control memory, explain in brief.

5 a) Explain the Stack Organization with example.
b) With a neat diagram explain floating point addition/subtraction unit.

6 a) Discuss the differences between RISC and CISC.
b) Write Booth multiplier recoding table. Perform booth multiplication on the following numbers -13(multiplicand), +11 (multiplier).

7 a) Draw the block diagram of a DMA controller and explain its functioning.
b) List the applications of Vector processing. Write in brief about vector operations.

8 **a)** List and explain different types of cache memory mapping techniques.
b) How address mapped using pages in virtual memory? Explain.

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R17

Code No: R17A0510

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech I Semester Supplementary Examinations, July/August 2021

Computer Organization

(CSE & IT)

Roll No										

Time: 3 hours **Max. Marks: 70**

Answer Any **Five** Questions
All Questions carries equal marks.

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1 a) What is the purpose of addressing modes? Explain various addressing mode techniques. **[7M]**

b) Design and explain 4-bit adder-subtractor and 4-bit arithmetic circuit to perform addition and subtraction using full adders. **[7M]**

2 a) Explain the complete design of simple system to implement RTL code using direct connections, bus and tri-state buffers. **[7M]**

b) Design the bus system for 4 registers and explain the working of it? **[7M]**

3 a) Explain the organizations of micro programmed control unit with neat sketch. **[7M]**

b) What is address sequencing? Explain the conditional branching and mapping of instruction in it. **[7M]**

4 a) Explain micro sequencer organization with a neat sketch. **[7M]**

b) Discuss the following:
Computer configuration for micro program, Symbolic micro program and binary micro program. **[7M]**

5 a) What are the different data transfer and data manipulation instructions and explain with example. **[7M]**

b) Design 4 bit Adder and Subtractor circuit and explain its operations. **[7M]**

6 a) Write the Division algorithm and explain with an example. **[7M]**

b) Differentiate CISC and RISC microprocessors? Explain the architecture of CISC and RISC microprocessors **[7M]**

7 a) Explain instruction execution in a 4 stage pipeline with flowchart. **[7M]**

b) What are the different major hazards in pipelined execution **[7M]**

8 a) Draw a neat block diagram of memory hierarchy in a computer system. Compare the parameters size, speed and cost per bit in the hierarchy. **[7M]**

b) Explain ROM and RAM with respect to their block diagrams **[7M]**

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R17

Code No: R17A0510

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech I Semester Supplementary Examinations, Dec-21/Jan-22

Computer Organization

(CSE & IT)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

1 Describe the functional blocks of a computer. Explain the RTL interpretation of instructions. **[14M]**

OR

2 Illustrate the various addressing modes of the CPU. Brief on fixed and floating point representation of relevant data. **[14M]**

SECTION-II

3 Describe the phases in Instruction cycle. **[14M]**

OR

4 Illustrate with a neat architecture about design of control unit **[14M]**

SECTION-III

5 Explain in detail about CISC and RISC machines **[14M]**

OR

6 Demonstrate with example the working of shift & add and booths multiplier. **[14M]**

SECTION-IV

7 Briefly describe the modes of data transfer in detail. **[14M]**

OR

8 List various parallel processing challenges. Draw the block diagram of 5 stage pipeline system. **[14M]**

SECTION-V

9 Explain briefly about Associate-mapped and set-associate mapped cache memory **[14M]**

OR

10 Describe about the segmented page mapping and page replacement in detail **[14M]**

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R17

Code No: R17A0510

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech I Semester Supplementary Examinations, February 2021

Computer Organization

(CSE & IT)

Roll No										

Time: 2 hours 30 min **Max. Marks: 70**

Answer Any **Five** Questions
All Questions carries equal marks.

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1 a) Explain various number systems and number representations used in system. **[7M]**

b) Dividend A=01110 Divisor B=10001. Explain flowchart for divide operation. **[7M]**

2 a) Convert the $(256)_{10}$ into following codes **[7M]**

i) Binary Coded Decimal (BCD) ii) Excess 3 codes

iii) Gray code iv) Reflected Code **[7M]**

b) Explain addition and subtraction algorithms for data represented in signed magnitude and signed 2's compliment.

3 a) What are the different phases a basic computer instruction cycle consists? Explain instruction cycle with flowchart. **[7M]**

b) a) Explain the design of control unit. How to decode the micro operation fields? Explain the process. **[7M]**

4 a) Write the format of the micro instruction and micro operations for the control memory. **[7M]**

b) With neat sketch explain the design of control unit of basic computer. **[7M]**

5 a) What are the different types of addressing modes and explain with examples **[7M]**

b) Write the multiplication algorithm and explain with an example **[7M]**

6 a) Draw the circuit for 4-Bit BCD Adder and explain its operations. **[7M]**

b) Explain the STACK Organization **[7M]**

7 a) Differentiate parallel processing and pipeline processing and explain them. **[7M]**

b) Explain arithmetic pipeline with example **[7M]**

8 a) What is virtual memory? With the help of neat sketch explain the method of virtual to physical address translation. **[7M]**

b) Explain the READ and WRITE operations in Associative Memory **[7M]**

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R17

Code No: R17A0510

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech I Semester Supplementary Examinations, May 2019

Computer Organization

(CSE & IT)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

1(a)	Explain in brief the evolution of computer generations.	**[7M]**
(b)	Differentiate between: (i) Input unit and Output unit (ii) Third generation & Fourth generation computers	**[7M]**
	OR	
2(a)	Explain the various input output modes of data transfer.	**[7M]**
(b)	Define micro operation? Explain arithmetic micro operations.	**[7M]**

SECTION-II

3(a)	Explain about the address sequencing in control memory. Draw the diagram to show selection of address that is to be loaded into the Control address register.	**[7M]**
(b)	Describe briefly about the register organization for floating point operations.	**[7M]**
	OR	
4(a)	Differentiate between Hard-wired controlled and Microprogrammed controlled microinstructions.	**[7M]**
(b)	Explain how to construct a common bus for four registers of n bits each using three state buffers.	**[7M]**

SECTION-III

5(a)	Explain Booth's multiplication algorithm with an example.	**[7M]**
(b)	Explain the following addressing modes with examples: (i) Immediate mode (ii) Relative mode (iii) Auto increment	**[7M]**
	OR	
6(a)	Discuss the Arithmetic operations on floating point numbers.	**[7M]**
(b)	With the help of suitable diagram, explain a circuit that can be used to perform either addition or subtraction of binary numbers.	**[7M]**

SECTION-IV

7	Write in detail about modes of I/O transfer.	**[14M]**
	OR	
8	Explain in detail about Asynchronous data transfer.	**[14M]**

SECTION-V

9(a)	Consider a memory consisting of 64K words of 8 bits each. Give the organization to implement this memory using 16K X 1 static memory chips.	**[7M]**
(b)	Construct an associative memory page table with number of words equal to the number of blocks in the main memory.	**[7M]**
	OR	
10(a)	Write a short note on virtual memory.	**[7M]**
(b)	Write short notes on a)magnetic Disks B) Magnetic tapes,	**[7M]**

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R17

Code No: R17A0510

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech I Semester Supplementary Examinations, November 2019

Computer Organization

(CSE & IT)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

1	a)	What are the different performance measures used to represent a computer system performance?	**[7M]**
	b)	Discuss about Error Detection codes.	**[7M]**
		OR	
2	a)	Explain Arithmetic, logic and shift micro-operations with examples.	**[10M]**
	b)	Describe single bus organization of a computer system.	**[4M]**
		SECTION-II	
3	a)	Explain role of different computer registers with respect to instruction Fetch cycle and execution. Give example.	**[7M]**
	b)	With the diagram explain the basic organization of micro programmed control unit.	**[7M]**
		OR	
4	a)	List the basic computer registers with their bit size, register name and functionality.	**[7M]**
	b)	Write the differences between Hardwired Control and micro programmed control.	**[7M]**
		SECTION-III	
5	a)	Explain basic instruction types. Give an example for each type.	**[7M]**
	b)	Explain addition and subtraction algorithm in computer arithmetic	**[7M]**
		OR	
6	a)	What is Addressing mode? Explain following addressing modes: i) Direct addressing mode ii) Indexed addressing mode iii) Auto increment addressing mode iv) Auto decrement addressing mode v) Indirect addressing mode	**[7M]**
	b)	Explain stack organization with block diagram.	**[7M]**
		SECTION-IV	
7	**a)**	Describe the different modes of transfer.	**[7M]**
	b)	What are the different stages of Instruction pipeline? Explain.	**[7M]**
		OR	
8	a)	Differentiate the Asynchronous and synchronous data transfers.	**[7M]**
	b)	What are the conflicts raised in pipelining? Suggest solutions to overcome these conflicts.	**[7M]**

SECTION-V

9	**a)**	What is cache memory? State different mapping techniques in detail	**[10M]**
	b)	What is page fault? What does page fault signifies when occurred. Explain page replacement algorithms.	**[4M]**
		OR	
10	**a)**	Explain the memory hierarchy with a neat diagram.	**[7M]**
	b)	Define hit rate and miss penalty. Calculate the total access time if miss rate is 0.12 miss penalty is 0.015ms and cache access time is 10microseconds.	**[7M]**

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R15

Code No: R15A0510

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech II Semester Supplementary Examinations, December 2019

Computer Organization

(CSE)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B
Part A is compulsory which carriers 25 marks and Answer all questions.
Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

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PART-A (25 Marks)

1). a	Define a Parity bit.	**[2M]**
b	Define a microoperation. Give examples	**[3M]**
c	What are the different phases in an instruction cycle	**[2M]**
d	What are the advantages and disadvantages of Hardwired Control Unit	**[3M]**
e	Define cache memory.	**[2M]**
f	Define an interrupt. What are the different types of interrupts	**[3M]**
g	Define a Peripheral. Give Examples	**[2M]**
h	What are the different conflicts in instruction pipelining	**[3M]**
i	Define locality of reference	**[2M]**
j	Draw the memory hierarchy diagram	**[3M]**

PART-B (50 MARKS)

SECTION-I

2	(a) What are the different functional units of a computer and explain	**[6M]**
	(b) Differentiate between multi processors and multi computers.	**[4M]**
	OR	
3	(a) List at least 8 logic microoperations	**[4M]**
	(b) Draw the circuit diagram of 4-bit adder-subtractor circuit and explain its operation	**[6M]**

SECTION-II

4	(a) List the various types of registers used in a basic computer and explain	**[4M]**
	(b) Explain the different instruction formats of a basic computer	**[6M]**
	OR	
5	(a) What are the address sequencing capabilities in a control memory	**[4M]**
	(b) Draw the Microinstruction format and explain each field	**[6M]**

SECTION-III

6	Define effective address? And Explain various addressing modes in detail with numerical examples.	**[10M]**
	OR	
7	(a) Write the three address instruction formats to evaluate X=(A+B)*(C+D)	**[4M]**
	(b) Explain the Stack organization in a system	**[6M]**

SECTION-IV

8 (a) What is the need of I/O interface module. Differentiate isolated IO and memory mapped I/O? **[5M]**

(b) Explain the concept of asynchronous data transfer. **[5M]**

OR

9 What is meant by instruction pipeline? Explain four segment Instruction Pipeline. Give its timing diagram **[10M]**

SECTION-V

10 (a) Write short note on Magnetic Disks **[3M]**

(b) What is virtual memory? With the help of neat sketch explain the method of virtual to physical address translation. **[7M]**

OR

11 (a) Explain how read and write operations are performed in Associative memory **[5M]**

(b) Explain Direct mapping technique used for cache mapping **[5M]**

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R15

Code No: R15A0510

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech II Semester Supplementary Examinations, February 2021

Computer Organization

(CSE)

Roll No										

Time: 2 hours 30 min **Max. Marks: 75**

Answer Any **Five** Questions

All Questions carries equal marks.

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1	Evaluate the following arithmetic statement using zero, one, two and three address instructions. Use the conventional symbols and instructions. X = (A+B) * (C+D).	**[15M]**
2	Draw a flowchart for adding and subtracting two fixed point binary numbers where Negative numbers are signed 1's complement presentation.	**[15M]**
3	With a neat Block Diagram explain about Input – Output and Interrupts	**[15M]**
4	Differentiate between hardwired control and micro programmed control. Is it possible to have a hardwired control associated with a control memory, Justify your answer	**[15M]**
5	a) Illustrate the different types of addressing modes with examples. b) Represent the following conditional control statement by two register transfer statements with control functions: If(P=1) then(R1←R2) else if (Q=1) then (R1←R3).	**[7M]** **[8M]**
6	Show the step-by-step multiplication process using Booth algorithm when the following binary numbers are multiplied. (+33) × (-12).	**[15M]**
7	Reproduce instruction pipeline with clear examples.	**[15M]**
8	Compare interrupt driven data transfer scheme and DMA. Using block diagram explain interrupt driven transfer scheme.	**[15M]**

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R15

Code No: R15A0510

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech II Semester Supplementary Examinations, June 2022

Computer Organization

(CSE)

Roll No										

Time: 3 hours **Max. Marks: 75**

Answer Any **Five** Questions
All Questions carries equal marks
***

1 List and explain the functional units of a computer. **[15M]**

2 List the registers for the basic computer and give their functionality in program execution. **[15M]**

3 Write a detailed note on instruction cycle. **[15M]**

4 Describe the micro programmed control organization and compare its advantages over hardwired control. **[15M]**

5 Explain Computer Arithmetic in detail. **[15M]**

6 Compare and Contrast CISC and RISC. **[15M]**

7 Analyze the parallel processing architecture and its uses. **[15M]**

8 Explain cache memory and cache coherence? **[15M]**

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R15

Code No: R15A0510

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech I Semester supplementary Examinations, May 2019

Computer Organization

(IT)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B
Part A is compulsory which carriers 25 marks and Answer all questions.
Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

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PART-A (25 Marks)

1). a	What is 2's compliment ? give examples.	**[2M]**
b	What is Register Transfer ? give example.	**[3M]**
c	What is Instruction cycle.	**[2M]**
d	Explain the different timing diagrams associated with buses.	**[3M]**
e	Write the advantages of RISC over CISC.	**[2M]**
f	What is Addressing mode ? List any 4 addressing modes.	**[3M]**
g	What is meant by pipelining and the advantage of pipelining.	**[2M]**
h	What are the functions of typical I/O interface.	**[3M]**
i	What is the function of TLB.	**[2M]**
j	Why does DMA have priority over the CPU when both requests a memory transfer.	**[3M]**

PART-B (50 MARKS)

SECTION-I

2	a) What are the design goals of Computer Architecture.	**[5M]**
	b) Explain about Floating-point representation.	**[5M]**
	OR	
3	Distinguish between error detection and error correction. Explain with an example how Hamming code is used for error detection.	**[10M]**

SECTION-II

4	a) Show how a 9-bit micro operation field instruction can be divided into subfield to specify 46 micro-operation. How many micro-operations can be specified in one micro instruction.	**[5M]**
	b) What is control field encoding ? Explain the role and advantages of micro programming.	**[5M]**
	OR	
5	a) Give the micro operations needed to execute the instruction LDA.	**[5M]**
	b) Write about Hardwired control	**[5M]**

SECTION-III

6	Explain in detail the principle of carry-look-ahead adder, Show how 16-bit CLA's can be constructed from 4-bit adders.	**[10M]**

OR

7 a) Distinguish between circular shift and arithmetic shift with example **[5M]**

b) Explain the three basic types of Data manipulation instructions **[5M]**

SECTION-IV

8 a) Explain the daisy chain mechanism of data transfer. **[5M]**

b) Explain briefly the purpose of an IO processor in data transfer between a peripheral device and CPU **[5M]**

OR

9 a) Explain pipeline chaining and vector loops in a vector processor. **[5M]**

b) Describe the implementation of multiply instruction use narrative and flowchart. **[5M]**

SECTION-V

10 a) Describe the concept of cache memory and explain the methods of writing into cache. **[5M]**

b) Explain the Memory Hierarchy. **[5M]**

OR

11 A Digital computer has a memory unit of 64 K x 16 and a cache memory of 1 K words. The cache uses direct mapping with a block size of four words. How many bits are there in the tag, index, block an word fields of the address format? How many blocks can the cache accommodate ? **[10M]**

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